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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,211	08/20/2003	Richard B. Brown	YOR920030266US1	5456

33233 7590 02/02/2005

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 02/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/644,211	BROWN ET AL.	
	Examin r	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *26-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-10,19-21 and 23-25* is/are rejected.

7)☒ Claim(s) *6,11-18 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

[redacted]

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-25, drawn to circuit, classified in class 326, subclass 33

II. Claims 26-29, drawn to designing a circuit, classified in class 716.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as apparatus and product made. The inventions in this relationship are distinct if either or both of the following can be shown: (1) that the apparatus as claimed is not an obvious apparatus for making the product and the apparatus can be used for making a different product or (2) that the product as claimed can be made by another and materially different apparatus (MPEP § 806.05(g)). In this case the product can be made by another and materially different apparatus (different circuits, switches).

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Charle Peterson on 1/26/05 a provisional election was made without traverse to prosecute the invention of I, claims 1-25. Affirmation of this election must be made by applicant in replying to this Office action.

Claims 26-29 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Morikawa (6,118,328).

1. Morikawa shows an integrated circuit (1C) comprising:

a plurality of functional units (inherent limitation, since all LSI includes a plurality of functional units in the circuit) selectively communicating with each other;

a plurality of logic circuits (10, 11, Fig. 1) connected together in ones of said plurality of functional units, connected said logic circuits in each of said ones defining function therein;

selectable supply switching devices (Q1) disposed at ones of said logic circuits selectively supplying power and alternately isolating connected said logic circuits, said selectable supply switching devices turning on at a threshold voltage having a magnitude greater (col. 2, lines 30-37) than like devices is said logic circuits, and

a switchable bias supply (12, 13) at each selectable supply switching device selectively reducing threshold voltage magnitude responsive to said each selectable supply switching device supplying power.

2. Morikawa shows the devices are field effect transistors (FETs), ones of said selectable supply switching devices are p-type FETS (Q1) connected between a supply line (Vdd) and an intermediate supply line.

3. Morikawa shows ones of said selectable supply switching devices are supplying power to said connected logic circuits, said switchable bias supply at said ones provides a body bias of Vdd - 0.7V to said one (col. 4, lines 21-37).

4. Morikawa shows ones of said selectable supply switching devices are isolating said connected logic circuits, said switchable bias supply at said ones provides a body bias of Vdd to said one (col. 3, line 20-40), whereby leakage current in and off said one is substantially reduced with said body bias of Vdd over said off ones with body bias at Vdd - O.7V (col. 4, lines 21-37).

5. Morikawa shows at least one said intermediate supply line (VVDD) is connected to two or more of said logic circuits (10, 11, and so on).

3. Claims 7-10, 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Notani (6,559,708).

7. Notani shows an integrated circuit comprising: a plurality of functional units (internal circuits and I/O buffer circuit, col. 11, lines 53-67) selectively communicating with each other;

a plurality of logic circuits (internal circuit 1, Fig. 1 and one of I/O buffer is considered as a functional unit) connected together in each of said plurality of functional units, connected said logic circuits in each functional unit defining function in said each unit; and

selectable supply switching devices (QA1-QA3 and QB1-QB3) disposed at ones of said logic circuits selectively alternately supplying power (VDD or GND) and isolating connected said logic circuits, said selectable supply switching devices being a high threshold device (col. 7, lines 30-37) turning on at a threshold voltage having a magnitude greater than at least one like devices is said logic circuits, each said of selectable supply switching devices being one in a series (QA3 and QA2) of stacked high threshold devices.

8-9. Notani shows devices are field effect transistors (FETs), ones of said selectable supply switching devices are p-type FETS (QA3) connected between a supply line (Vdd) and other (QA2) connected to an intermediate supply line.

10. Notani shows at least one the intermediate supply is connected to two or more the logic circuits (internal circuits, Fig. 1 & Fig. 3 connect to I/O buffer circuit).

19-20. Notani shows the devices are field effect transistors (FETs), ones of said selectable supply switching devices are n-type FETS (QB3) connected between a supply return line (GND) and other (QB2) connected to an intermediate return line.

21. Notani shows at least one the intermediate return is connected to two or more of the logic circuits (internal circuits, Fig. 1 & Fig. 3 connect to I/O buffer circuit).

Claim Rejections - 35 USC § 103

4. Claims 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Notani (6,559,708).

5. Notani discloses the claimed invention except for the widest high threshold devices being disposed in the series nearest to a logic circuit output and the narrowest at supply connections and high threshold devices being 4 times wider than its next adjacent narrower stacked device. It would have been an obvious matter of design choice to provide the widest high threshold devices being disposed in the series nearest to a logic circuit output and the narrowest at supply connections and high threshold devices being 4 times wider than its next adjacent narrower stacked device, since such a modification would have involved a mere change in the size and location of a component. A change in size and rearranging parts of an invention involves only routine skill in the art.

Allowable Subject Matter

6. Claims 6, 11-18, 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Makino (6,242,949) and Yamagata et al (5,726,946) disclose circuit device having switching elements for stand-by mode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

2/1/05